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RFLM-501202MC-299

RFuW Engineering Pte. Ltd.

Passive High Power Two Stage Passive Limiter Module - SMT

Features:

- Frequency Range: 250 MHz to 3.5 GHz
- Average Power: +45 dBm
- Peak Power: +54 dBm
- Insertion Loss: <0.4 dB
- Return Loss: >18 dB
- Flat Leakage Power: <21dBm
- Spike Energy Leakage: 0.3 ergs
- Recovery Time: 500 nsec
- Package: 8mm x 5mm x 2.5mm
- No external control lines or power supply required
- RoHS Compliant

Description:

The RFLM-501202MC-299 SMT Silicon PIN Diode Limiter Module offer both High Power CW and Peak Power protection in the 250 MHz to 3.0 GHz frequency range. It is based on a proven hybrid assembly technique utilized extensively in high reliability, mission critical applications. The RFLM-501202MC-299 offers excellent thermal characteristics in a compact, low profile 8mm x 5mm x 2.5mm package. The RFLM-501202MC-299 is designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering excellent large input signal Flat Leakage for effective receiver protection in the 250 MHz to 3.5 GHz frequency range.

The limiter RF circuit characteristics provide outstanding passive receiver protection (always on) which protects against High Average Power up to +45 dBm, High Peak Power up to +54 dBmpulsed (pulse width = 1 usec, duty cycle = 0.1%), maintains low flat leakage to less than +21 dBm (typical),and reduces Spike Leakage to less than 0.3 ergs.

ESD and Moisture Sensitivity Rating

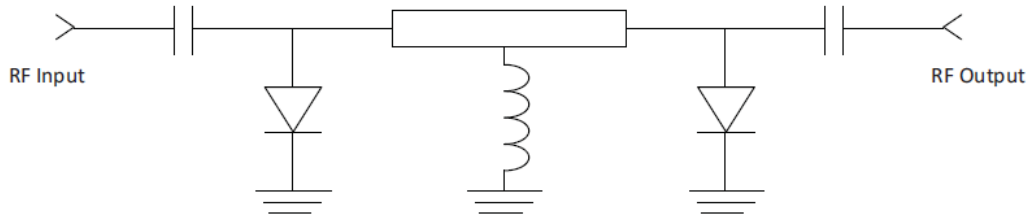
The RFLM501202MC-299 Limiter Module carries a Class 1C ESD rating (HBM) and an MSL 1 moisture rating.

Thermal Management Features

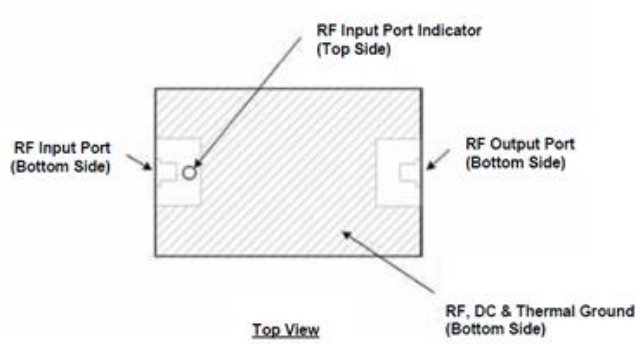
The RFLM-501202MC-299 based substrate has been design to offer superior long term reliability in the customer's application by utilizing ultra-thin Au plating to combat Au embrittlement concerns. Also, a proprietary design methodology has minimized the thermal resistance from the PIN Diode junction to base plate. The two

stage limiter design employs a second stage limiter and quarter wavelength spacer detector circuit which permits ultra-fast turn on of the High Power PIN Diodes. This circuit topology coupled with the thermal characteristic of the substrate design enables reliably handling High Input RF Power up to +45 dBm CW and RF Peak Power levels up to +54 dBm (1 uSec pulse width @ 0.1% duty cycle with base plate temperature at +85°C).

RFLM-501202MC-299 Limiter Module Schematic - with RF Coupling Capacitors



Pin Out



Absolute Maximum Ratings

@ Zo=50Ω, T_A= +25°C as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65°C to 125°C
Storage Temperature		-65°C to 150°C
Junction Temperature		175°C
Assembly Temperature	T = 30 seconds	260°C
RF Peak Incident Power	T_{CASE}=85°C, source and load VSWR < 1.2, RF Pulse width = 1 usec, duty cycle = 0.1%, derated linearly to 0 W at T_{CASE}=150°C (See note 1)	+54 dBm
RF CW Incident Power		+45 dBm
Assembly Temperature		260°C for 30 seconds

Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

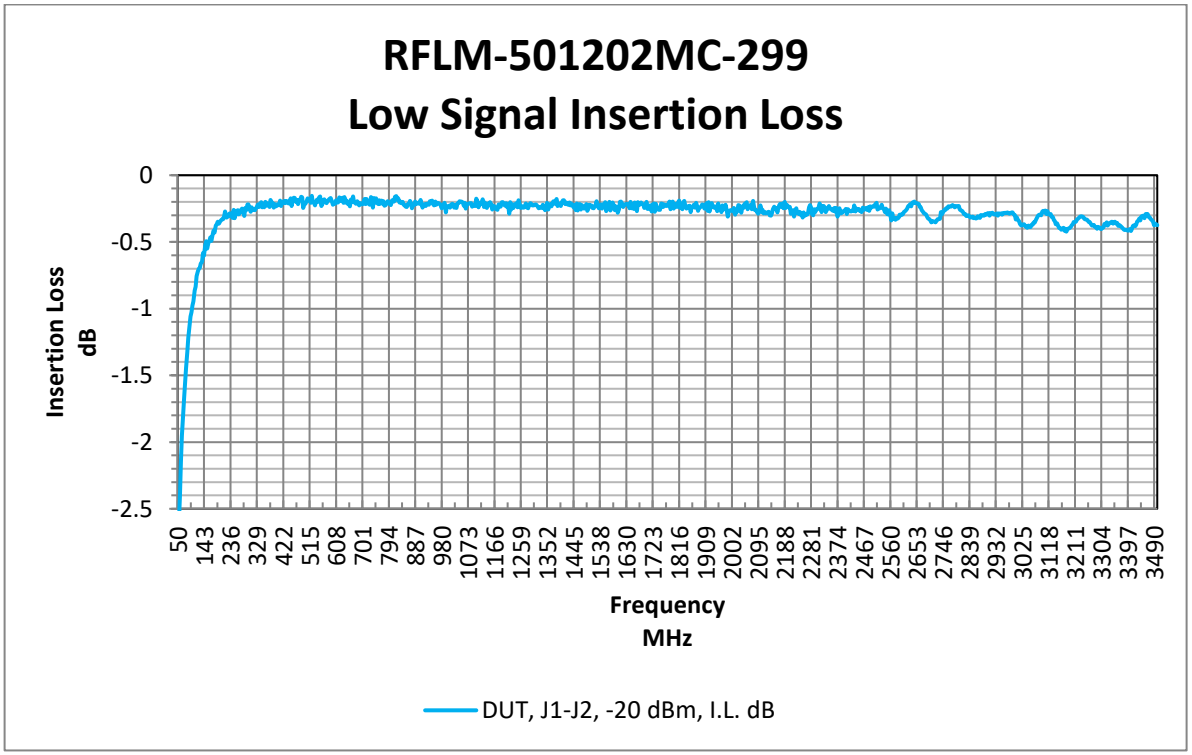
RFLM501202MC-299 Electrical Specifications

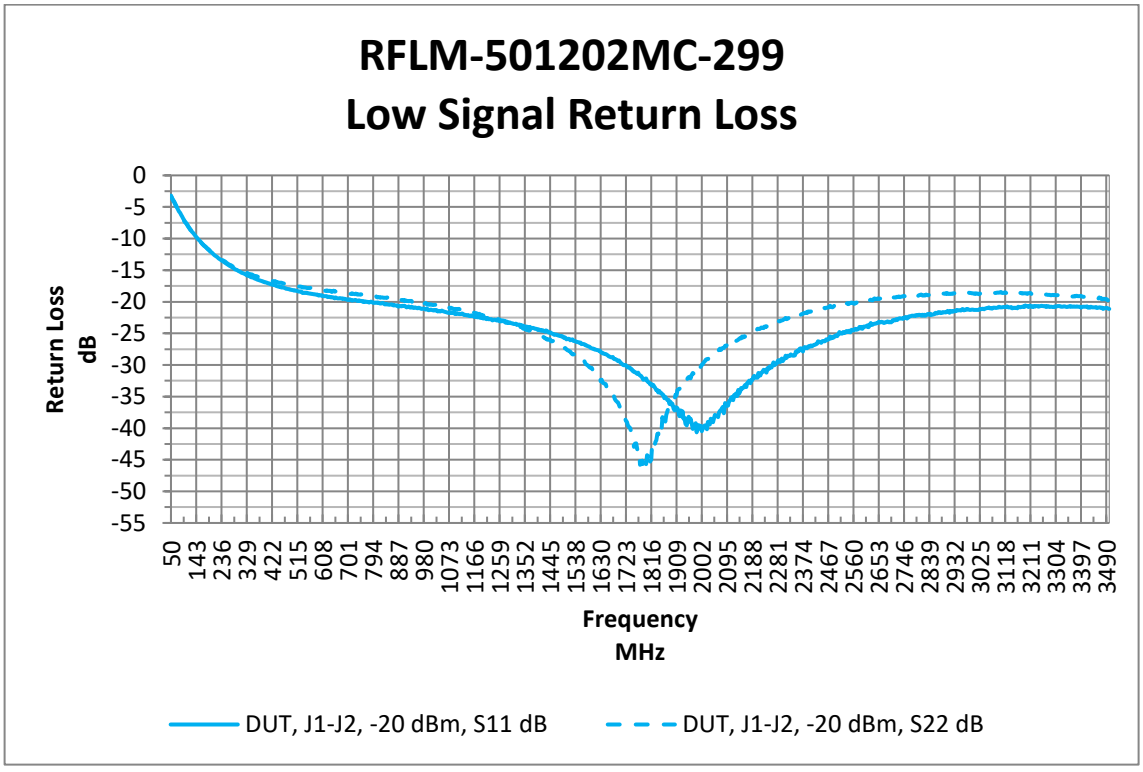
@ Zo=50Ω, TA= +25°C as measured on the base ground surface of the device.

Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F		0.25		3.5	GHz
Insertion Loss	IL	400 MHz ≤ F ≤ 2.5 GHz, P_{in}= -10 dBm		0.4	0.6	dB
Insertion Loss Rate of Changevs Operating Temperature	ΔIL	400 MHz ≤ F ≤ 2.5 GHz, Pin ≤ -10 dBm		0.005		dB/°C
Return Loss	RL	400 MHz ≤ F ≤ 2.5 GHz, Pin= -10 dBm	18	20		dB
Input 1 dB Compression Point	IP_{1dB}	400 MHz ≤ F ≤ 2.5 GHz		8		dBm
2nd Harmonic	$2F_o$	P_{in}= 0 dBm, F_o= 2.0 GHz	-45	-50		dBc
Peak Incident Power	$P_{inc\ (PK)}$	RF Pulse = 1 usec, duty cycle = 0.1%, t_{rise} ≤ 2us, t_{fall} ≤ 2 usec			54	dBm
CW Incident Power	$Pi_{nc(CW)}$	400 MHz ≤ F ≤ 2.5 GHz			45	dBm
Flat Leakage	FL	P_{in} = 50 dBm, RF Pulse width = 1 us, duty cycle = 0.1%, t_{rise}≤ 2 us, t_{fall}≤ 2 us		21	22	dBm
Spike Leakage	SL	Pin = 50 dBm, RF Pulse width = 1 us, duty cycle = 0.1%			0.3	erg
Recovery Time	T_R	50% falling edge of RF Pulse to 1 dB IL, Pin = 50 dBm peak, RF PW = 1 us, duty cycle = 0.1%, trise ≤ 2us, t_{fall} ≤ 1 usec		500	750	nsec

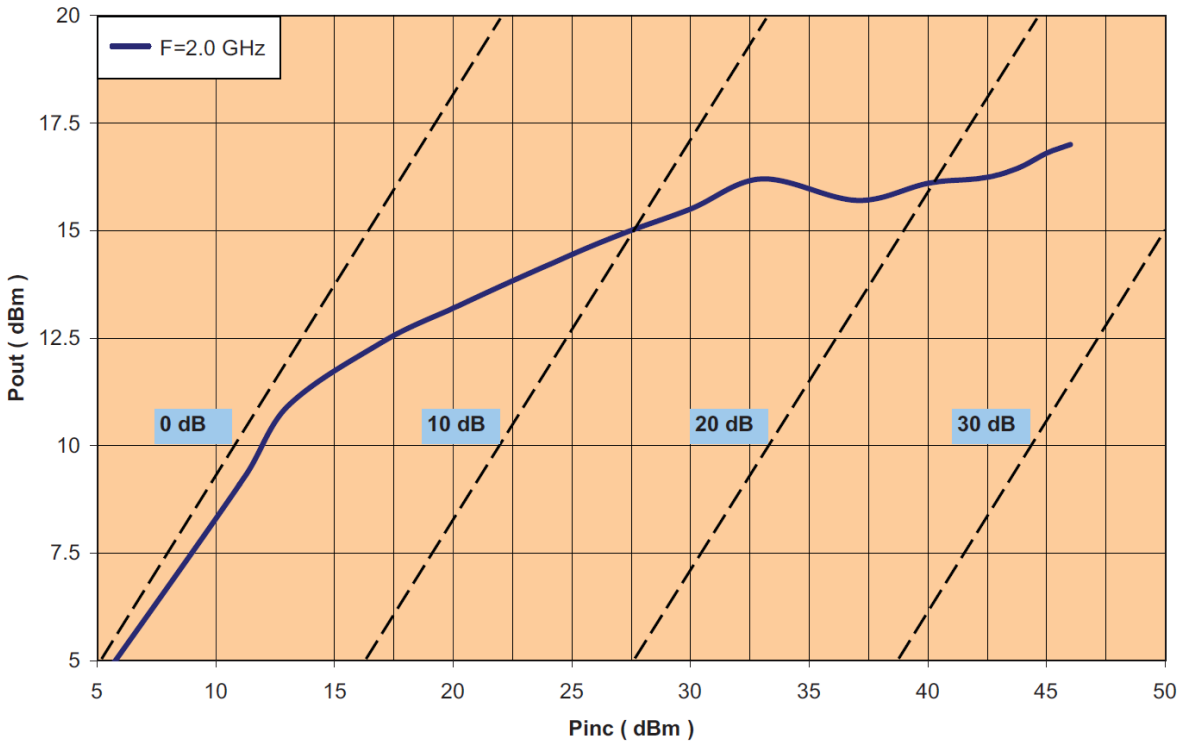
RFLM-501202MC-299 Typical Performance

Z_o = 50Ω, T_{CASE} = 25°C, PIN = -20 dBm as measured on the Ground Plane of the device.





RFLM-501202MC-299 Flat Leakage: Peak Power P_{out} vs P_{in}

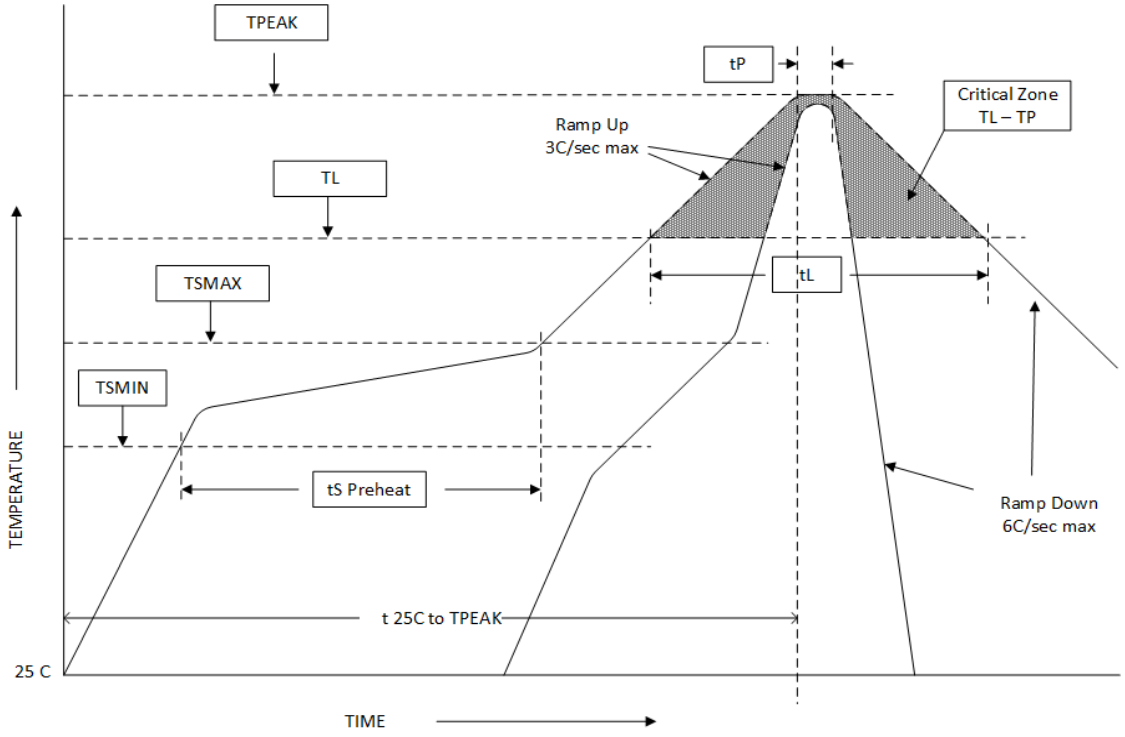


Assembly Instructions

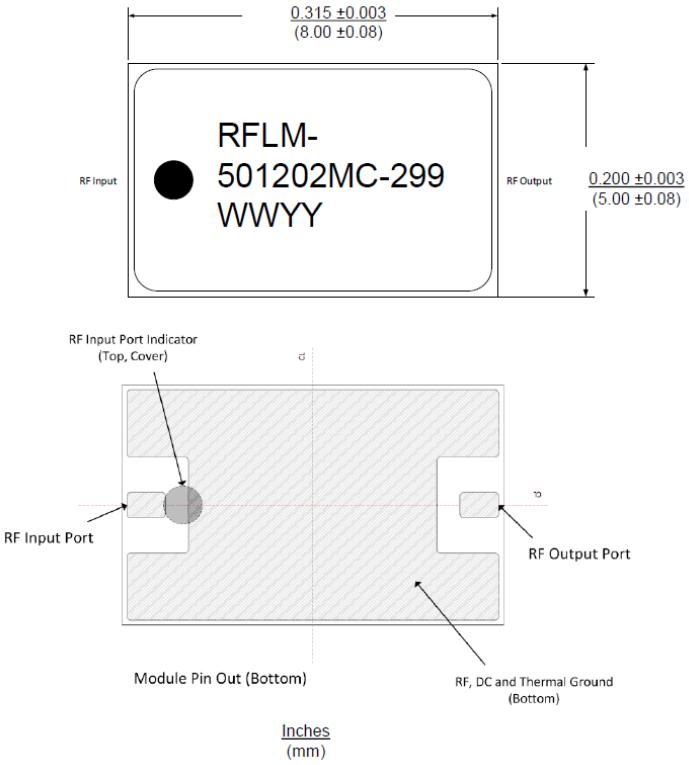
The RFLM-501202MC-299may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T_L to T_P)	3°C/sec (max)	3°C/sec (max)
Preheat Temp Min (T_{smin}) Temp Max (T_{smax}) Time (min to max) (t_s)	100°C 150°C 60 – 120 sec	100°C 150°C 60 – 120 sec
T_{smax} to T_L Ramp up Rate		3°C/sec (max)
Peak Temp (T_P)	225°C +0°C / -5°C	245°C +0°C / -5°C
Time within 5°C of Actual Peak Temp (T_P)	10 to 30 sec	20 to 40 sec
Time Maintained Above: Temp (T_L) Time (t_L)	183°C 60 to 150 sec	217°C 60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to T_P	6 minutes (max)	8 minutes (max)

Solder Re-Flow Time-Temperature Profile



RFLM-501202MC-299 Limiter Module Package Outline Drawing



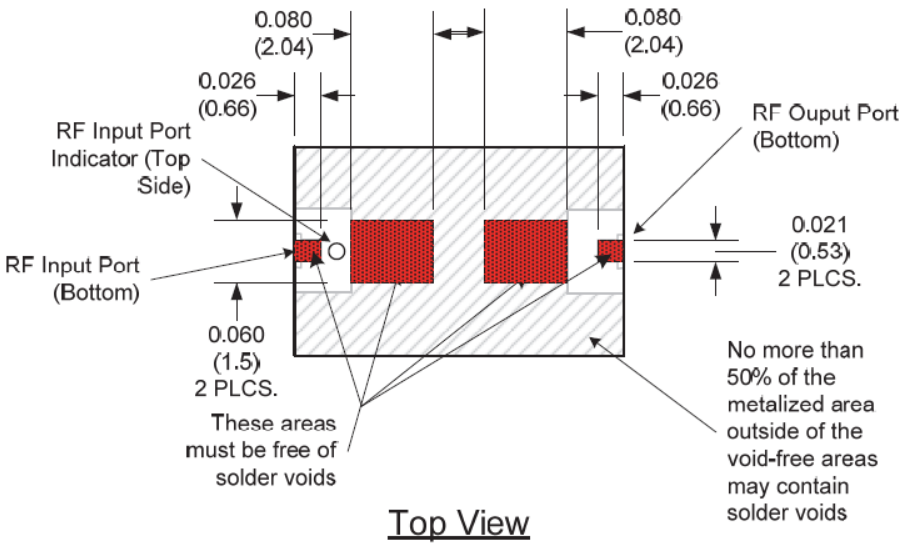
Notes:

1) Metalized area on backside is the RF, DC and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
2) Back side metallization is thin Au termination plating to combat Au embrittlement (15 u in typ Au plated over Ti-Pd).

Thermal Design Considerations:

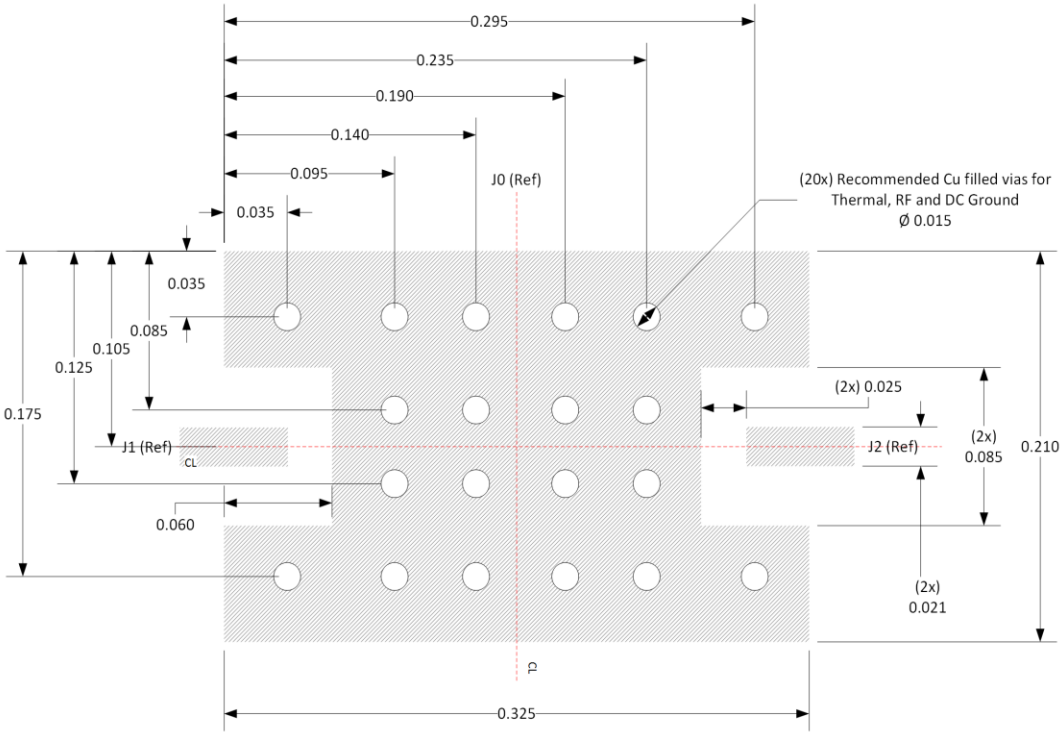
The design of the RFLM-501202MC-299 Limiter Module permits the maximum efficiency in thermal management of the PIN Diodes while maintaining extremely high reliability. Optimum Limiter performance and reliability of the device can be achieved by the maintaining the base ground surface temperature of less than 85°C.

There must a minimal thermal and electrical resistance between the limiter and ground. Adequate thermal management is required to maintain a T_{jc} at less than +175°C and therefore will not adversely affect the semiconductor reliability. Special care must be taken to assure that minimal voiding occurs in the solder connection in the areas shade in red in the figure shown below.



Dimensions in inches (mm).

Recommended RF Circuit Solder Footprint for the RFLM501202MC-299



Notes:

1) Recommended PCB material is rogers 4350, 10 mils thick.
2) Hatched area is RF, DC and Thermal Ground. Vias should be solid Cu filled and Au plated for optimal heat transfer from backside of Limiter Module through circuit vias to thermal ground.

Part Number Ordering Detail:

The RFLM-501202MC-299 Limiter Module is available in the following format.

Part Number	Description	Packaging
RFLM-501202MC-299	250 MHz to 3.5 GHz Band Limiter (SMT)	Gel Pack
RFLM-501202MC-299 SS EVB	RFLM-501202MC-299 Small Signal Evaluation Board	Box
RFLM-501202MC-299 HP EVB	RFLM-501202MC-299 High Power Evaluation Board	Box
RFLM-501202MC-299C	RFLM-501202MC-299 SMA Connectorized High Power Limiter	Box